Properties of Ta–Mo alloy gate electrode for *n*-MOSFET

CHUNG KEUN LEE*, JAE YOUNG KIM, SHIN NAM HONG
School of Electronic Engineering, Telecommunication and Computer Engineering, Hankuk Aviation University, 200-1, Hwajon-dong, Deokyang-gu, Koyang-City, Kyonggi-do 412-791, Korea
E-mail: cklee@eeabyss.hangkong.ac.kr

HUICAI ZHONG
Advanced Micro Devices, Hopewell Junction, NY 12533, USA

BEI CHEN, VEENA MISRA
Department of Electrical and Computer Engineering, North Carolina State University, Raleigh, NC 27695, USA

As complementary metal oxide semiconductor (CMOS) devices are scaled beyond the 50-nm gate length node, the effective oxide thickness must be below 10 Å to reduce short-channel effect and to improve device performance. Polysilicon has been extensively employed as a gate electrode, however, it has recently shown to suffer from instability on high-K dielectrics [1]. In addition, the inversion oxide thickness is increased by about 3–5 Å due to polysilicon gate depletion [2]. Based on the above reasons, the investigation of metal gates is critical for scaling of advanced gate stacks [3].

Metal gate electrodes must have suitable work function, process compatibility and thermal/chemical interface stability with underlying gate dielectrics. In order to replace the polysilicon gate while maintaining the proper threshold voltage, work functions of the metal gates for n-channel MOS (NMOS) and p-channel MOS (PMOS) must be close to those of n^+ and p^+ doped polysilicon, which are close to 4 and 5 eV, respectively [4]. Metals with mid-gap work functions are known to be unsuitable for advanced CMOS devices due to severely degraded short channel characteristics [5].

While several thermally stable metals have been reported as possible gate electrodes for PMOS devices [6], metals having NMOS compatible work function typically suffer from thermal instability. Their high affinity towards oxygen promotes the reduction of the underlying dielectric and the formation of a metal oxide layer [7]. Binary metal alloys have been recently reported [6] and may provide a possible route for NMOS electrodes. In this work, we have investigated the electrical/material properties and thermal stability of a novel binary metal alloy, Ta–Mo, for NMOS gate electrode.

Field oxide of 3500 Å was grown to define active area on (100) p-type silicon substrate. The gate dielectric was 100 Å SiO_2 which was thermally grown at 900 □. The binary metal alloys were deposited using a UHV-PVD sputtering tool with a base pressure of 3×10^{-9} Torr. Sputtering was performed using a Ta target (purity of 99.5%) and a Mo target (purity of 99.95%). As shown in Table I, the powers of the two targets were adjusted to obtain alloys with varying compositions.

The thickness of the Ta–Mo binary alloy gates was ∼500 Å and the gates were patterned by lift-off process. All samples were then rapid thermal annealed (RTA) in Ar ambient at 600 □, 700 □, 800 □, and 900 □ for 10 s to ascertain the thermal properties of the alloys. Capacitance-voltage (C-V) and current-voltage (I-V) were obtained using HP 4280 LCR meter (1 MHz) and HP 4155 semiconductor parameter analyzer, respectively. Sheet resistances were measured using a 4-point probe. Flat-band voltage (V_{FB}) and effective oxide thickness were extracted using a quantum model [8].

Fig. 1 shows the atomic percent of Ta and Mo measured by field emission scanning electron microscopy (FESEM). Ta-rich film was obtained even when the percent of Ta sputtering power was far less than that of Mo.

Fig. 2 shows C-V characteristics of all samples after RTA at 600 □, for 10 s. The flat-band voltages shift to positive values as the Ta composition decreases, which indicates that the work functions of metal gates is changing as a function of the alloy composition. In order to obtain the appropriate work function, varying thicknesses of gate dielectric must be used. Although, in this work, only one thickness is used, the V_{FB} trends suggest that the work function trends are also similar.

Fig. 3 shows the variation of flat-band voltage as the Ta power changes. Flat-band voltage varies between −0.75 and −0.21 V. These values of flat-band voltage suggest that low work function is obtained when the percent of Ta sputtering power is higher than 50%. The most NMOS compatible V_{FB} values were obtained when the percent of Ta power was 58.8% (atomic percent of 90.7%).

The reported sheet resistance of polysilicon is about 80–300 Ω/□ [9]. When the Ta atomic composition was 90.7%, the measured sheet resistance of Ta–Mo alloy after 600 □ RTA was about 16 Ω/□. Since the sheet resistance of Ta–Mo alloy is very low, the alloy can be used as a gate electrode of a low power device. After 600 □ RTA, the leakage current of capacitor with Ta–Mo

*Author to whom all correspondence should be addressed.

0022–2461 © 2005 Springer Science + Business Media, Inc.

TABLE I List of sputtering power conditions

Sample number	Ta power (W)	Mo power (W)	Ta power (%)
1	100	30	76.9
2	100	70	58.8
3	100	100	50.0
4	70	100	41.2
5	30	100	23.1
6	0	100	0.0

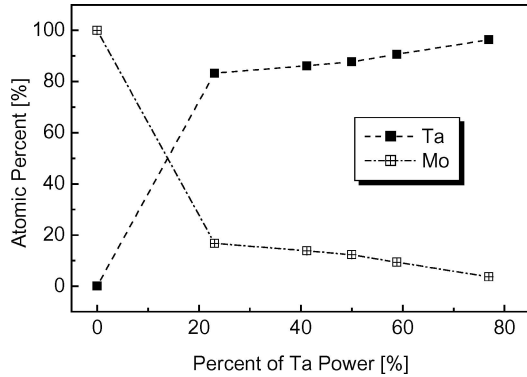

Figure 1 Composition of Ta–Mo alloys as a function of Ta power.

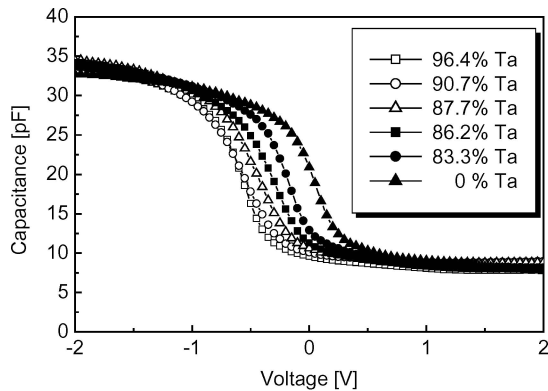

Figure 2 C-V curves showing the dependence of flat-band voltage on the composition of Ta–Mo alloy.

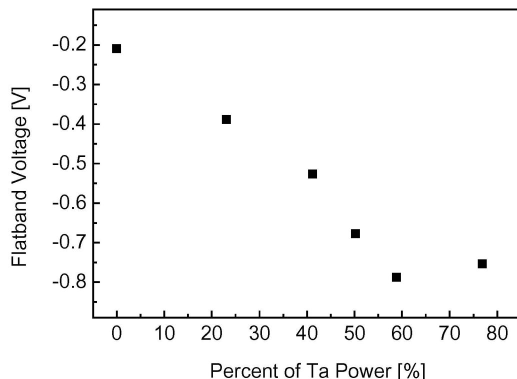

Figure 3 Flatband voltage extracted from C-V curves for various percent of Ta power.

alloy electrode that has 90.7% Ta atomic composition is about 4.2×10^{-12} A at $V_g = -4$ V.

The thermal stability between metal film and dielectric can be judged by the formation of interface layer and the change of flat-band voltages. To identify thermal stability, MOS capacitors with alloy electrode of

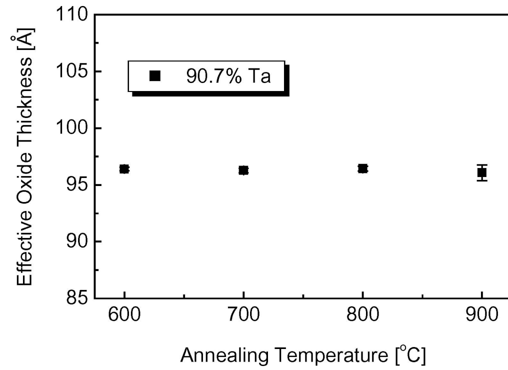

Figure 4 The change of gate dielectric thickness after various annealing temperatures.

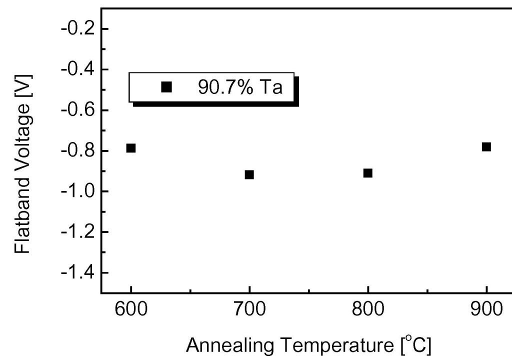

Figure 5 The change of flatband voltage after various annealing temperatures.

90.7% Ta atomic composition were rapid thermal annealed in Ar at 600 □, 700 □, 800 □, and 900 □ for 10 s.

Figs 4 and 5 show the effective oxide thickness and flat-band voltage measurement results. As can be seen in Fig. 4, the difference of effective oxide thickness between the two capacitors annealed at 600 □ and 900 □ is 0.33 Å. This indicates that the interface layer is almost not formed between metal and dielectric after 900 □ RTA. The variation of flat-band voltage after 900 □ annealing is 0.007 V as shown in Fig. 5. This change is negligibly small. The leakage current increases about 10 pA after 900 □ annealing, but this increase does not greatly affect the device operation. The Ta–Mo alloy with 90.7% of Ta atomic composition can be considered to be thermally stable, since there are very little changes of effective oxide thickness and flat-band voltages up to 900 □ RTA.

In conclusion, Ta–Mo alloy metal gate was deposited by co-sputtering technique. Co-sputtering enables the easy control of the composition of alloy by varying the relative sputtering power of each component. Flat-band voltage was dependent on the composition of alloy. When the atomic composition of Ta was 90.7%, flat-band voltages obtained were appropriate for NMOS. Pure Ta gate was reported to be unstable with the underlying gate oxide if the processing temperature of over 700 □ was employed [10]. But Ta–Mo alloy was very stable up to 900 □. Since the binary alloy of Ta and Mo provides the appropriate flat-band voltage and correspondingly the appropriate work function, it is suitable for the gate electrode of NMOS devices.

Acknowledgment
This work was supported by the Korea Ministry of Science & Technology under Grant No. R05-2004-000-11226-0. Sample fabrication was carried out at NCSU Microelectronics Laboratory. The authors thank Diana Hong for her assistance in measurements and manuscript preparation.

References
1. C. HOBBS, L. FONSECA, V. DHANDAPANI, S. SAMAVEDAM, B. TAYLOR, J. GRANT, L. DIP, D. TRIYOSO, R. HEGDE, D. GILMER, R. GARCIA, D. ROAN, L. LOVEJOY, R. RAI, L. HEBERT, H. TSENG, B. WHITE and T. TOBIN, *Symp. of VLSI Technol.* (2003) 9.
2. Y. TAUR, D. A. BUCHANAN, W. CHEN, D. J. FRANK, K. E. ISMAIL, S. H. LO, G. A. SAI-HALASZ, R. G. VISWANATHAN, H. J. C. WANN, S. J. WIND and H. S. WONG, *Proc. IEEE* **85** (1997) 486.
3. Semiconductor Industry Association, 2000 update.
4. I. DE, D. JOHRI, A. SRIVASTAVA and C. M. OSBURN, *Solid State Electron.* **44** (2000) 1077.
5. B. CHENG, M. CAO, R. RAO, A. INANI, P. V. VOORDE, W. M. GREEN, J. M. C. STOCK, Z. YU, P. M. ZEITZOFF and J. C. S. WOO, *IEEE Trans. Electron. Devices.* **46** (1999) 1537.
6. H. ZHONG, GREG HEUSS and V. MISRA, *Appl. Phys. Lett.* **78** (2001) 1134.
7. V. MISRA, G. P. HEUSS and H. ZHONG, *ibid.* **78** (2001) 4166.
8. J. R. HAUSER and K. AHMED, *Nat. Inst. Stand. Technol.* (1998).
9. J. E. SUAREZ, B. E. JOHNSON and B. EL-KARCH, *IEEE Trans. Comon. Hybrids Manuf. Technol.* **15** (1992) 537.
10. T. USHIKI, M. C. YU, Y. HIRANO, H. SHIMADA, M. MORITA and T. OHMI, *IEDM* (1996) 117.

Received 17 June
and accepted 14 October 2004